REMARKS

As a preliminary matter, the specification is objected to for the reasons set forth on pages 2-3 of the present Office Action. Applicant amends the specification, as indicated in herein, and Applicant believe that these proposed amendments obviate the Examiner's objection to the specification.

Claims 1-7 are all the claims pending in the present application. Claims 1 and 2 are rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. Claims 1-7 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Applicant admitted prior art (APA) in view of Gupte et al. (US Patent No. 5,812,416).

§112 Rejections - Claims 1 and 2

Claims 1 and 2 are rejected under 35 U.S.C. § 112, second paragraph, for the reasons set forth on page 3 of the present Office Action. Applicant amends claims 1 and 2, as indicated herein, and Applicant believes that these amendments obviate the Examiner's rejections of claims 1 and 2 under 35 U.S.C. § 112, second paragraph.

§103(a) Rejections (APA / Gupte) - Claims 1-7

Claims 1-7 are rejected for the reasons set forth on pages 4-6 of the present Office Action. Applicant traverses these rejections at least based on the following reasons.

With respect to independent claims 1 and 2, the Examiner believes that the APA satisfies the preambles of these claims; however the Examiner acknowledges that the APA does not disclose or suggest each and every feature set forth in claims 1 and 2. The Examiner, however, believes that Gupte makes up for the deficiencies of the APA. With respect to claim 1, Applicant submits that the applied references, either alone or in combination, do not disclose or

suggest at least, "storing said register properties in a data-structure according to said structure of said hardware device, said register properties being arranged in an array for each module or dependent sub-module." In the Office Action, the Examiner alleges that Gupte discloses a data structure of testing the ASIC and storing the properties of the ASIC in a module and dependent sub-module pattern, however nowhere does the Examiner mention and nowhere do the applied references disclose that the registered properties are arranged in an array for each module or dependent sub-module.

Yet further, Applicant submits that the applied references do not disclose or suggest that the registered properties in the data structure are stored according to the structure of the hardware device. The Examiner acknowledges that the APA does not disclose this particular feature, and the Examiner does not even argue that Gupte satisfies this particular feature.

Therefore, at least based on the foregoing, Applicant submits that independent claim 1 is patentably distinguishable over the combination of the APA and Gupte, either alone or in combination. Applicant submits that independent claim 2 is patentable at least based on reasons similar to those set forth above.

Applicant submits that dependent claims 3-7 are patentable at least by virtue of their ultimate dependencies from independent claim 2.

Further, with respect to claim 3, the Examiner alleges that the features set forth in this claim are inherent, and further notes, "that the repetition indicators are embedded features or part of the tree data structure in link-listed algorithm, which includes head and tail as indicators to indicate the beginning, next, and the end of the pre-data structure." In response, Applicant submits that, even if, *arguendo*, a link-listed algorithm includes head and tail indicators of

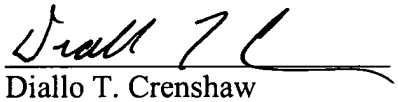
beginning, next, and end of the tree data structure, nowhere do either of the applied references disclose or suggest the specific feature of an array corresponding to a module of a hardware device comprising a number of repetitions indicator, adapted to indicate the number of reoccurrences of a submodule of a module. Therefore, at least based on the foregoing, Applicant submits that claim 3 is patentably distinguishable over the applied references.

Further, with respect to claims 6 and 7, Applicant submits that the particular feature of the data structure being used in access test executed by a generic test device, is not satisfied by either of the applied references. The Examiner believes that Gupte satisfies this specific feature, however nowhere does this reference disclose that a data structure is used as an access test executed by a generic test device. Further, with respect to claim 7, even if, *arguendo*, Gupte does describe an access test executed by a generic test device, nowhere does Gupte disclose or suggest that such test include one of read/write of multiple patterns to two registers, a data-bus test, an address-bus test, and a device reset test or a test of initial values of all registers, as recited in claim 7. Figure 5 and the cited portions of Gupte do not even discuss an access test or the specifics of said access test. At least based on the foregoing, Applicant submits that claims 6 and 7 are patentable over the applied references.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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